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SPI "system packet interface"

- 2003

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[CITATION] **System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical and Link Layer ...**

R Cam, R Tuck - OPTICAL INTERNETWORKING FORUM, January, 2001

[Cited by 7](#) - Related articles - Web Search

[Implementation of 10gigabit packet switching using IXP network processors](#)

C Sheng, Z Xu, C Yingxin, D Wei - Communication Technology Proceedings, 2003. ICCT 2003. ..., 2003 - ieeexplore.ieee.org

... external interfaces: Receive and transmit interfaces, each of which can be individually configured for either the **SPI-4 Phase 2 (System Packet Interface)** to a ...

[Cited by 4](#) - Related articles - Web Search

[An implementation of protocol converter for RPR \(resilient packet ring\) module](#)

SW Lee, HS Lee, HH Lee, DY Kim - Communications, 2003. APCC 2003. The 9th Asia-Pacific ..., 2003 - ieeexplore.ieee.org

... descrambling function. The processed packet is transferred to SRP MAC with

SPI-3 (System Packet Interface -3) interface. 2.2 SRP MAC ...

[Cited by 3](#) - Related articles - Web Search

[Design and development of the first single-chip full-duplex OC48 traffic manager and ATM SAR SoC- ► cadence.com \[PDF\]](#)

A Khan, K Patel, A Aurora, A Raza, B Parruck, A ... - Custom Integrated Circuits Conference, 2003. Proceedings of ..., 2003 - ieeexplore.ieee.org

... 11.2. IC Architecture This open architecture device [I] connects simultaneously with standard **system packet interface 4.2 (SPI-4.2)** and packet over synchronous ...

[Cited by 4](#) - Related articles - Web Search - BL Direct - All 5 versions

[Analysis of a QoS-based parallel packet switch for core routers](#)

W Li, Y Gong, B Liu - Communication Technology Proceedings, 2003. ICCT 2003. ..., 2003 - ieeexplore.ieee.org

... (64bits/200MHz, **System Packet Interface Level 4**) [8] as its front interface, whose bandwidth is four times the rate of back interface (32bits1100MHz). ...

[Cited by 3](#) - Related articles - Web Search

[CITATION] **System Packet Interface Level 3**

R Cam... - SPI-3 specification Optical Interface Forum, 2000

[Cited by 1](#) - Related articles - Web Search

[Optical networking module including protocol processing and unified software control](#)

IC Denton, B Murdock, JL Gimlett, EL Hershberg, SW ... - US Patent App. 10/414,115, 2003 - Google Patents
... to Point Protocol SDH Synchronous Digital Hierarchy SONET Synchronous Optical network, a PHY telecommunication protocol **SPI-4 System Packet Interface Level 4** ...[Cited by 4](#) - Related articles - Web Search - All 6 versions

[CITATION] **Physical layer solution for very short reach application utilizing parallel optics**

S Hart, A Technologies - 2002 - ONIDS

[Cited by 1](#) - Related articles - Web Search

[A scalable 10 Gb/s line-rate router with DiffServ support](#)

Y Xu, Z Dai, B Liu, W Li - Communication Technology Proceedings, 2003. ICCT 2003. ..., 2003 - ieeexplore.ieee.org

... A. Bur Interface Module (BIM) BIM completes the wnvlesion between interior data bus and **SPI-4 bus (System Packet Interface Level 4)**, which defines the data ...

[Cited by 1 - Related articles - Web Search](#)

DC offset cancellation circuit, system and method

S Seetharaman, K Kiziloglu, CW Abidin, GS Asmanis - US Patent App. 10/324,983, 2002 - Google Patents
... In other embodiments, such a backplane interface may comprise any one of several versions of the **System Packet Interface (SPI)** as defined by the Optical ...

[Cited by 1 - Related articles - Web Search - All 4 versions](#)

[\[PDF\] ► Jitter-Variations in the significant instants of a clock or data signal](#)

A Lesea - Xilinx TechXclusives Forum, 2001 - xilinx.com

... This range of possible test conditions can be used for a **System Packet Interface Level 4 Phase 2 (SPI-4.2) Packet-Over SONET/SDH Level 4 (POS-PHY L4)** design. ...

[Cited by 2 - Related articles - View as HTML - Web Search - All 2 versions](#)

[\[PDF\] ► Optical Transport Networks](#)

U Kumar, A Engineer, Z Semiconductor - IIC-China/ESC China 2002 Conference Proceedings, 2002 - eetasia.com

... The **System Packet Interface (SPI)** which is defined by OIF(Optical Internetworking Forum) defines an interface between Physical layer device and the link layer ...

[Cited by 2 - Web Search](#)

[\[CITATION\] All SPI-4s are not created equal-Phase 2 of the **System Packet Interface-4** is emerging as the new ...](#)

M Berry - EDN-BOSTON THEN DENVER THEN HIGHLANDS RANCH CO-, 2003 - CAHNERS PUBLISHING
[Web Search - BL Direct](#)

System packet interface

AB Evans, MI Tatar, CK Begin - US Patent App. 10/458,357, 2003 - Google Patents

... [0006] One commonly-utilized board-level interface is the **SPI-4.2 system packet interface** described by the Optical Internetworking Forum in "System Packet ...

[Web Search - All 6 versions](#)

Efficient non-user data transmission method

L Friesen, RJ Johnson, J Sterne, JM Schriehl, D ... - US Patent App. 10/316,946, 2002 - Google Patents

... The **SPI 4.2 protocol** is a **system packet interface** created by the Optical Internetworking Forum (OWF). [0005] In the prior art system shown in FIG. ...

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Semiconductor intellectual property and system-on-chip for communications the future for small ...

Z Nozica, LS Inc, CA San Jose - Telecommunications, 2003. ConTEL 2003. Proceedings of the ..., 2003 - ieeexplore.ieee.org

... process utilization (lowest cost): Full support of all EDA views for easy integration

System Packet Interface Level 4 (SPI-4) System Packet Interface Level 4 ...

[Related articles - Web Search](#)

Hypertransport/SPI-4 interface supporting configurable deskewing

LR Moll, M Gulati - US Patent App. 10/742,060, 2003 - Google Patents

... 8,2004 (54) HYPERTRANSPORT/SPI-4 INTERFACE SUPPORTING CONFIGURABLE DESKEWING (76)
Inventors: Laurent R. Moll, Saratoga, CA (US); Manu Gulati, San Francisco, CA ...

[Web Search - All 2 versions](#)

System interface for cell and/or packet transfer at aggregate data rates of up to 10 Gb/s

R Cam, JR Hamstra, W Mok, D Wong - US Patent App. 09/756,680, 2001 - Google Patents

... 4 illustrates the **SPI-4 FIFO status indication**; [0025] FIG. ... 6. POS-PHY Level 4 is the **system packet interface** for data transfer between the link layer and the ...

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Distributed copies of configuration information using token ring

L Moll, JB Rowlands - US Patent App. 10/684,909, 2003 - Google Patents

... eg, PCI (peripheral component interface) bus, ISA (industry standard architecture) bus, USB (universal serial bus), and **SPI (system packet interface)**. ...

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Multiple processor integrated circuit having configurable packet-based interfaces

B Sano, L Moll, M Gulati, J Keller - US Patent App. 10/356,390, 2003 - Google Patents

Page 1. US 20040019704A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0019704 A1 Sano et al. (43) Pub. Date: Jan. ...

[Web Search - All 2 versions](#)

Configurable transmit and receive system interfaces for a network device

E Lecha, C Calderon, J Gonzalez - US Patent App. 10/282,453, 2002 - Google Patents

... and/or receive packets of information, such as variable size Internet Protocol

(IP) packets in accordance with a **System Packet Interface (SPI)** as defined in ...

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Optimized data path structure for multi-channel management information base (MIB) event generation

S Ni - US Patent App. 10/090,845, 2002 - Google Patents

... In a channelized switch system, such as a **SPI-4 (System Packet Interface Level 4)** interface, generating MIB events becomes a nontrivial task. ...

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Bandwidth allocation fairness within a processing system of a plurality of processing devices

M Gulati - US Patent App. 10/356,346, 2003 - Google Patents

Page 1. US 20040030799A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0030799 A1 Gulati (43) Pub. Date: Feb. ...

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Hypertransport exception detection and processing

JB Rowlands, L Moll - US Patent App. 10/684,953, 2003 - Google Patents

... eg, PCI (peripheral component interface) bus, ISA (industry standard architecture) bus, USB (universal serial bus), and **SPI (system packet interface)**. ...

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System having two or more packet interfaces, a switch, a shared packet DMA (Direct Memory Access) ...

BJ Sano, LR Moll, K Oner, M Gulati - EP Patent 1,313,273, 2003 - freepatentsonline.com

... 4 wherein one of the two or more interfaces is a **system packet interface**. ... some embodiments, the interfaces may be system packet interfaces (**SPI**) according to ...

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System and method for efficient handling of network data

O Uzrad-Nali, S Gupta - US Patent App. 10/014,602, 2001 - Google Patents

... In yet another alternate implementation a **System Packet Interface Level 3 (SPI-3)** or a System Packet Physical Interface Level 4 (**SPI-4**) may be used. ...

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Transmitting data from a plurality of virtual channels via a multiple processor device

M Gulati, L Moll, J Keller - US Patent App. 10/356,348, 2003 - Google Patents

... device then packetizes, during a 4th transmission cycle, the stored data in accordance with a 1st or 2nd transmission protocol (eg, HT, **SPI**, et cetera) to ...

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Multi-service packet network interface

JMG Patenaude - US Patent App. 10/349,248, 2003 - Google Patents

Page 1. US 20040076166A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0076166 A1 Patenaude (43) Pub. Date: Apr. ...

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Circuit and method for processing communication packets and valid data bytes
AP Annadurai, F Han, M Rahman, C Tsu - US Patent App. 10/087,228, 2002 - Google Patents
... traffic. The framer communicates with the processor through an inter- face
known as the **SPI-4 (system packet interface)**. The **SPI** ...

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Smart routing between peers in a point-to-point link based system

M Gulati - US Patent App. 10/421,988, 2003 - Google Patents
Page 1. US 20030217177A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2003/0217177 A1 Gulati (43) Pub. Date: Nov. ...

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Simplifying verification of an SFI converter by data format adjustment

S Goyal, J Parvereshi - US Patent App. 10/373,265, 2003 - Google Patents
... 1, there are two (2) electrical interfaces within a SONET/SDH based communication
sys- tem: **system packet interface ("SPI")** 110 and SERDES framer interface ...

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Bridges performing remote reads and writes as uncacheable coherent

JB Rowlands - US Patent App. 10/685,136, 2003 - Google Patents
... eg, PCI (peripheral component interface) bus, ISA (industry standard architecture)
bus, USB (universal serial bus), and **SPI (system packet interface)**. ...

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System to provide fractional bandwidth data communications services

MD Scholten - US Patent App. 10/092,064, 2002 - Google Patents
... a given link layer device and the physical layer device are described in the Optical
Internetworking Forum standard **System Packet Interface (SPI)** level-4 ...

[Web Search](#) - All 4 versions

Apparatus and method to receive and align incoming data in a buffer to expand data width by

...
M Gulati, LR Moll - US Patent App. 10/685,231, 2003 - Google Patents
... Communi- cation technologies are typically based on certain commu- nicating protocols,
such as **SPI (system packet interface)** and hypertransport (HT) based ...

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Multi-service channelized sonet mapper framer

JG Patenaude - US Patent App. 10/318,468, 2002 - Google Patents
... eight 10-megabit-per-second (Mbps) or 100 Mbps Ethernet ports, two gigabit-per-second
(Gbps/GbE/Gig-E) Ethernet links, and **System Packet Interface (SPI-3) (POS)** ...

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Flow control interface

J Tierney, D Stuart, B Venables - US Patent App. 10/745,270, 2003 - Google Patents
... The **System Packet Interface (SPI)** defines how data packets are transferred between
a physical layer device (using a physical layer protocol) and a data link ...

[Web Search](#) - All 2 versions

Alignment and deskew device, system and method

H Woelk, A Fischer, N Hoffmann - US Patent App. 10/150,369, 2002 - Google Patents
... Also, the Optical Internetworking Forum (OIF) defines System Packet Interfaces
(SPIs) at Levels SPI-1 through SPI-5 for different data rates. ...

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Free packet buffer allocation

PR Chandra, U Naik, A Kumar, AS Varde - US Patent App. 10/668,550, 2003 - Google Patents
... embodiments, the communication interface device may be a Serial Peripheral Interface
(SPI) device 160 in accordance with the **System Packet Interface Level Four** ...

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Packet data recovery system

GR McLeod - US Patent App. 10/448,008, 2003 - Google Patents

... [0005] As an example, a bus standard that provides such flexibility is the **System Packet Interface Level 4 Phase 2 (SPI-4 Phase 2)** bus standard specification ...

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Method and apparatus for transmission on a 2-bit channel using 3b/4b code

JL Calvignac, JJ Lynch, DJ Sucher, FJ Verplancken - US Patent App. 10/096,161, 2002 - Google Patents

... Details of the **SPI-4** interface is set forth in the OIF document titled: "**System Packet Interface Level 4 (SPI-4) Phase 2: OC-192 System Interface for Physical** ...

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Multi-protocol networking processor with data traffic support spanning local, regional and wide area ...

C Denton, JL Gimleit - US Patent App. 09/860,207, 2001 - Google Patents

... Point to Point Protocol SFD Starting Frame Delimiter SONET Synchronous Optical network, a PHY telecommunication protocol **SPI-4 System Packet Interface Level 4** ...

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Efficient routing of packet data in a scalable processing resource

B Sano, L Moll, M Gulati - US Patent App. 10/356,323, 2003 - Google Patents

Page 1. US 20040030712A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2004/0030712 Al Sano et al. (43) Pub. Date: Feb. ...

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Message transfer system

A Lines, C Stoops, E Peterson, A Gravel - US Patent App. 10/452,782, 2003 - Google Patents

... extender interface 108, a JTAG/EJTAG interface 110, a general purpose input/output (GPIO) interface 112, and a **System Packet Interface Level 4 (SPI-4) Phase** ...

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Robust and scalable de-skew method and apparatus for data path skew control

JM Chiang - EP Patent 1,355,465, 2003 - freepatentsonline.com

... 1. **SPI-4** is the **system packet interface** for data transfer between the link layer and the PHY device; it is designed to meet requirements of this particular ...

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Method and apparatus utilizing a tail bus to solve back-to-back data burst problems

NY Chu, JM Chiang - US Patent App. 10/269,989, 2002 - Google Patents

... 1, system 100 may include an interface 103 between an external device 102 and an internal device 105, which may be a **SPI-4 (System Packet Interface Level 4** ...

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Method and apparatus for unscheduled flow control in packet form

EG Chen, R Cherukuri, R Wadhawan - US Patent App. 10/021,152, 2001 - Google Patents

... Internetworking Forum **System Packet Interface Level 4 Phase 2: OC-192 System Interface for Physical and Link Layer Devices** (January 2001) (the "OIF **SPI-4.2.2** ...

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Traffic management using in-band flow control and multiple-rate traffic shaping

KS Grant, MB Simkins, DP Sonnier - US Patent App. 10/689,090, 2003 - Google Patents

... an interface stan- dard, such as the **SPI-3** interface standard described in Implementation Agreement OIF-SPI3-0 1.0, "**System Packet Interface Level 3 (SPI-3)**: ...

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Data path optimization algorithm

SH Ni - US Patent App. 09/982,794, 2001 - Google Patents

... in applications such as aggre- gating multiple-Gigabit ports to an uplink interface back- plane such as a **System Packet Interface Level 4 (SPI-4) Phase 2** ...

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Fastpath implementation for transparent local area network (LAN) services over multiprotocol label ...

L Shankar, S Ambe - US Patent App. 10/377,664, 2003 - Google Patents

... For example in the embodiment of FIG. 5, the physical port may be an interface such as a **System Packet Interface Level 4 (SPI-4)** port channel. ...

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Interconnecting network processors with heterogeneous fabrics

G Lebizay, DW Gish, NC Oliver - US Patent App. 10/313,783, 2002 - Google Patents

... Interface for Physical and Link Layer Devices," dated June 2000 ("SPI-3 Specification"), the OIF document titled "**System Packet Interface 4 (SPI-4) Phase 2: OC** ...

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Switch operation scheduling mechanism with concurrent connection and queue scheduling

L Moll - US Patent App. 10/685,376, 2003 - Google Patents

Page 1. US 20040078459A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2004/0078459 Al Moll (43) Pub. Date: Apr. ...

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Packet data service over hyper transport link (s)

M Gulati, L Moll, B Sano - US Patent App. 10/356,661, 2003 - Google Patents

Page 1. US 20040037313A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2004/0037313 Al Gulati et al. (43) Pub. Date: Feb. ...

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Determining a checksum from packet data

J Krueger - US Patent App. 10/692,585, 2003 - Google Patents

Page 1. US 20050089031A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2005/0089031 Al Krueger (43) Pub. Date: Apr. ...

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Laser driver circuit and system

AA Krishnaswami, T Yoon - US Patent App. 10/742,377, 2003 - Google Patents

... In other embodiments, such a backplane interface may comprise any one of several versions of the **System Packet Interface (SPI)** as defined by the Optical ...

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A method and apparatus for solving data burst problems using two buses

NY Chu, JM Chiang - EP Patent 1,345,128, 2003 - freepatentsonline.com

... 1, system 100 may include an interface 103 between an external device 102 and an internal device 105, which may be a **SPI-4 (System Packet Interface Level 4** ...

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Data link/physical layer packet diversion and insertion

DR Primrose, IC Denton - US Patent App. 09/918,691, 2001 - Google Patents

... SDH Synchronous Digital Hierarchy SONET Synchronous Optical network, a PHY telecommunication protocol SOP Start of Packet **SPI-4 System Packet Interface Level** ...

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Packet assembly

PR Chandra, S Lakshmanamurthy, CC Kuo, R Natarajan ... - US Patent App. 10/742,189, 2003 - Google Patents

Page 1. US 20050135353A1 (19) United States (12) Patent Application Publication

(io> Pub. NO.: US 2005/0135353 Al Chandra et al. (43) Pub. Date: Jun. ...

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Processing instructions

EJ Johnson, JL Jason, SD Goglin - US Patent App. 10/641,614, 2003 - Google Patents

... The processor 200 can also feature an interface 202 (eg, a **System Packet Interface Level 4 (SPI-4) interface**) that enables the processor 200 to communicate ...

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Centralized switching fabric scheduler supporting simultaneous updates

L. Moll, M Gulati - US Patent App. 10/684,915, 2003 - Google Patents

... CELLS switching module 51 TRANS. CELLS *••4 HyperTransport/ **SPI-4/PCI/etc.** ... Rx MAC
66 Tx MAC 68 (Agent B) (Agent B) HyperTransport/ **SPI-4/PCI/etc.** ...

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System and method for providing isolated fabric interface in high-speed network switching and

... SA Sarkinen, JD Swart, NA Schlegel, JM Meyer, DL ... - US Patent App. 09/995,410, 2001 - Google Patents

... Another such standard is the Optical Internetworking Forum (OIF) **System Packet Interface-4 (SPI-4)** which describes a data path interface between the physical ...

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Dynamic resource allocation systems and methods

VK Balakrishnan - US Patent App. 10/719,469, 2003 - Google Patents

... for transmitting packets to other processor(s) or circuitry connected to the fabric;
an interface 105 (eg, a **System Packet Interface Level 4 (SPI-4)** interface ...

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Link layer device with configurable address pin allocation

AQ Khan, DB Kramer - US Patent App. 10/744,567, 2003 - Google Patents

... an interface stan- dard, such as the **SPI-3** interface standard described in
Implementation Agreement OIF-SPI3-01.0, "System Packet Interface Level 3 (**SPI-3**): ...

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Apparatus and method for header processing

SH NI - EP Patent 1,313,291, 2003 - freepatentsonline.com

... be employed in applications such as aggregating multiple-Gigabit ports to an uplink
interface backplane such as a **System Packet Interface Level 4 (SPI-4)** Phase ...

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Protocol data unit queues

D Romano, G Wolrich, DF Hooper - US Patent App. 10/460,289, 2003 - Google Patents

... The processor 200 can also feature an interface (eg, a **System Packet Interface Level 4 (SPI-4)** interface) that enables to the processor 200 to communicate with ...

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Network statistics

S Jain, DF Hooper - US Patent App. 10/628,997, 2003 - Google Patents

... The processor 200 can also feature an interface 202 (eg, a **System Packet Interface Level 4 (SPI-4)** interface) that enables to the processor 200 to communicate ...

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Laser driver circuit and system

BS Asuri, T Yoon - US Patent App. 10/442,829, 2003 - Google Patents

... In other embodiments, such a backplane interface may comprise any one of several
ver- sions of the **System Packet Interface (SPI)** as defined by the Optical ...

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Laser driver circuit and system

V Magooon - US Patent App. 10/193,354, 2002 - Google Patents

... In other embodiments, such a backplane interface may comprise any one of several
versions of the **System Packet Interface (SPI)** as defined by the Optical ...

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Coprocessor bus architecture

ND McDonnell - US Patent App. 10/403,428, 2003 - Google Patents

... may be associated with other protocols, including Internet Protocol (IP) packets
exchanged in accor- dance with a **System Packet Interface (SPI)** as defined in ...

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Controlling access to sections of instructions

DF Hooper, A Kumar - US Patent App. 10/445,168, 2003 - Google Patents

... The processor 500 can also feature an interface 502 (eg, a **System Packet Interface Level 4 (SPI-4) interface**) that enables the processor 500 to communicate ...

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Data alignment systems and methods

CM Lin - US Patent App. 10/749,328, 2003 - Google Patents

... for transmitting packets to other processor(s) or circuitry connected to the fabric; an interface 105 (eg, a **System Packet Interface Level 4 (SPI-4) interface**) ...

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Storage registers for a processor pipeline

ND McDonnell, J Wishneusky - US Patent App. 10/419,435, 2003 - Google Patents

... ments may be associated with other protocols, including Internet Protocol (IP) packets exchanged in accordance with a **System Packet Interface (SPI)** as defined ...

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Inserting instructions

EJ Johnson, JL Jason, HM Vin - US Patent App. 10/734,457, 2003 - Google Patents

Page 1. US20060212874A1 (19) United States (12) Patent Application Publication GO

Pub. No.: US 2006/0212874 Al Johnson et al. (43) Pub. Date: Sep. ...

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Multi-service Ethernet-over-SONET silicon platform

JG Patenaude - US Patent App. 10/318,444, 2002 - Google Patents

... device. An Optical Interface Forum **System Packet Interface** compliant interface is not used in an embodiment of the present invention. ...

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Generating packets

CE Narad - US Patent App. 10/722,727, 2003 - Google Patents

... performed by the Rx MAC 222, the framer 120 can output the resulting packet via an interface 232, such as a **System Packet Interface** (eg an SPI Level-n interface ...

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Management of received data within host device using linked lists

M Gulati, LR Moll - US Patent App. 10/675,745, 2003 - Google Patents

... BUS I/F (HT) Tx processing device A Tx Rx PKT I/F (**SPI-4**) processing device C FIG. ... o B 2 2 p o" CTQ fD ffl HyperTransponV **SPI-4/PCI/etc.** ...

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Distributed 4-bits diagonal interleaved parity (DIP4) checker

NY Chu - US Patent App. 10/234,165, 2002 - Google Patents

... Sheet 2 of 15 US 2003/0182613 Al Chip Boundary 110 J r 130 ^ ncrtir?'01 rctl - eg en | 3 rdat[15:0] - 2xrclk rclk PLL ^pi xclk ^125 External 16 bit **SPI-4** data ...

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Transimpedance amplifier with receive signal strength indicator

S Seetharaman, K Kizilloglu - US Patent App. 10/645,003, 2003 - Google Patents

... In other embodiments, such a backplane interface may comprise any one of several versions of the **System Packet Interface (SPI)** as defined by the Optical ...

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System and method of annotating network packets

EJ Johnson, AR Kunze, DM Putzolu, TA Anderson - US Patent App. 10/133,125, 2002 - Google Patents

... For example, the links 112 may comprise a UTOPIA bus or versions of the **System Packet Interface (SPI)** link defined by the Optical Internetworking Forum (OIF ...

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Stall optimization for a processor pipeline

ND McDonnell, J Wishneusky - US Patent App. 10/419,360, 2003 - Google Patents
Page 1. US 20040210740A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2004/0210740 Al McDonnell et al. (43) Pub. Date: Oct. ...

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Thread-based engine cache partitioning

S Lakshmanamurthy, WY Liao, PR Chandra, JY Mih, Y ... - US Patent App. 10/704,431, 2003 - Google Patents
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(io> Pub. NO.: US 2005/0102486 Al Lakshmanamurthy et al. (43) Pub. ...

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Apparatus and method for allocating resources within a security processing architecture using

...
MR Hussain, PH Dickinson, I Badr - US Patent App. 10/411,944, 2003 - Google Patents
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(io> Pub. NO.: US 2005/0060558 Al Hussain et al. (43) Pub. Date: Mar. ...

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Laser driver circuit

V Magoon - US Patent App. 10/645,143, 2003 - Google Patents
... In other embodiments, such a backplane interface may comprise any one of several
ver- sions of the **System Packet Interface (SPI)** as defined by the Optical ...

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Multi-service queuing method and apparatus that provides exhaustive arbitration, load
balancing, and ...

SA Sarkinen, SA Davidson - US Patent App. 09/957,751, 2001 - Google Patents
Page 1. US 20030058880A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2003/0058880 Al Sarkinen et al. (43) Pub. Date: Mar. ...

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Multi-service telecommunication switch

JP Jones, MP Demilia, RM Parker, MH Duymazlar - US Patent App. 10/277,023, 2002 - Google Patents
Page 1. US 20030081540A1 (19) United States (12) Patent Application Publication
(io> Pub. NO.: US 2003/0081540 Al Jones et al. (43) Pub. ...

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Programmable multi-service queue scheduler

SA Sarkinen, SA Davidson - US Patent App. 09/957,750, 2001 - Google Patents
... transferred to the ingress processing circuit 214 via an interface 216, such as
the Optical Internetworking Forum (OIF) **System Packet Interface-4 (SPI-4)**. OIF ...

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